Amendments to the Specification:

Please replace the paragraph beginning at page 18, line 24 with the following amended paragraph:

First, a sampling pulse is output from the shift register 5002 in sequence according to the timing at which a clock signal, a clock inverted signal and a start pulse are input. The sampling pulse is input to the data latch circuit ~~5004~~5003. The data latch circuit ~~5004~~5003 is reset by the sampling pulse which is input from the D-FF 5001 of the preceding stage, and then samples a digital video signal at the timing at which a sampling pulse from the D-FF 5007 of the present stage is input, thereby holding it. This operation is performed from the first column in sequence.